Claims 2, 8, 9, and 11 were rejected under 35 U.S.C. 112, second paragraph. Claims 2 and 8 have been amended.

Claim 2 was rejected under 35 U.S.C. 103(a) as being unpatentable over Hobbs et al. Applicants traverse the rejection. The claimed invention provides remarkable effects over the prior art in its capability on suppressing diffusion of impurities into the gate insulation film (see Figs. 2-9). Diffusion of impurities into the gate insulation film becomes a very serious concern as the gate insulation film gets thinner, e.g., at less than 2 nm.

The present inventors have discovered that when a gate electrode having Ru or Ir is used in combination with the TiO2 gate insulation film, a gate structure is provided with remarkable characteristics in suppressing diffusion of impurities (see Figs. 2-7). Such characteristics become particularly important for transistors having gate insulation films of 2 nm or less. The devices having such thin insulation films cannot be reliably operated if there is significant diffusion of impurities into the gate insulation films. The claimed invention solves this problem and enables the semiconductor technology to continue providing smaller and smaller devices.

In addition, the inventors have discovered that the diffusion prevention characteristics can be improved even more by using the TiO2 gate insulation film with specific crystal types of Ir or Rr gate electrode.

Hobbs discloses many kinds of materials, e.g., silicon oxide film, silicon nitride flim, and so on, for gate insulation material. However, Hobbs does not disclose the combination of Ti02 insulation film and Ir or Ru electrode, as recited in claim 1 and other claims. In addition, Hobbs is directed to a thick gate oxides, 2-5 nm, for which impurity diffusion is of less concern. Accordingly, Hobbs does not teach the claimed invention which is directed to a device for suppressing the diffusion of impurities into the gate insulation film, in the manner recited. Claim 2 is allowable.

Claims 1, 4-7, 12, and 13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hobbs et al. and in view of Tsunashima et al. Applicants traverse the rejection. Tsunashima discloses a device having a thin gate insulation film. However, Hobbs does not disclose and is not directed to thin film technology, as explained above. Therefore, the

two references could not be combined together to obtain the remarkable diffusion suppression capability of claim 1 as well as that of other claims. That is, Tsunashima discloses a device stack having ZrSiO, ZrO, TiN, and W; however, the mode and the material of Tsunashiam are different from those of the claimed invention. Claims 1, 4-7, 12, and 13 are allowable.

Claims 8, 9, and 11 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hobbs et el al. in further in view of Gilbert et al. Gilbert does not remedy the deficiency of Hobbs et al as set forth above. Claims 8, 9, and 11 are allowable.

Claim 10 was rejected under 35 U.S.C. 103(a) as being unpatentable over Hobbs et al. in combination with Gilbert and further in view of Tsunashiam. Applicants traverse the rejection. Claim 10 depend from claim 8 and is allowable at least for this reason.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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